End Semester Examination 2013-14
CSE, III Yr. (I Sem),
30002: Computer Organization

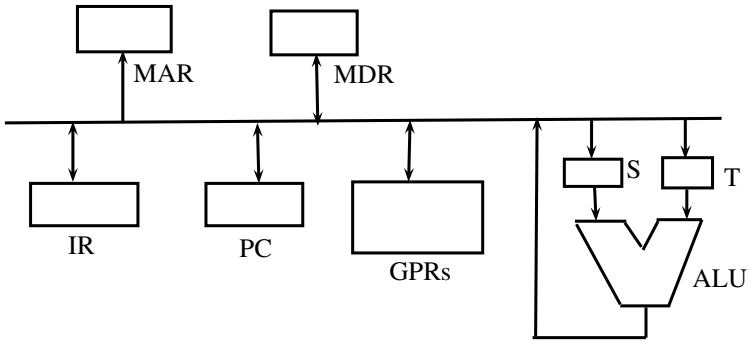
GROUP -A

Instructions:

1. Write the question paper group **(A, B, C, D)**, on front page top of answer book, as per what is mentioned in the question paper.
2. Attempt all questions.
3. Write the correct choice a, b, c, or d in answer book, for multiple choice questions (MCQs).
4. Wrong answer for an MCQ carries $-\frac{1}{4}$ of its full weightage.
5. Except MCQs, give the detailed answer/solution for each question.

Max. Marks=40 Time= 3 Hrs.

1. (a) The ALU, S, T, the bus and all the registers in the data path are of identical size. All operations including incrementation of the PC and the GPRs (general purpose registers) are to be carried out in the ALU. Two clock cycles are needed for memory read operation – the first one for loading address in the MAR and the next one for loading data from the memory bus into the MDR. (next two questions)



i. The instruction "add R0, R1"has the register transfer interpretation $R0 \leftarrow R0 + R1$. The minimum number of clock cycles needed for execution cycle of this instruction is: (2)
(a) 2 (b) 3 (c) 4 (d) 5

ii. The instruction "call Rn, sub"is a two word instruction. Assuming that PC is incremented during the fetch cycle of the first word of the instruction, its register transfer interpretation is

$$Rn <= PC + 1;$$
$$PC <= M[PC];$$

The minimum number of CPU clock cycles needed during the execution cycle of this instruction is: (2)
(a) 2 (b) 3 (c) 4 (d) 5

(b) i. A CPU has 24-bit instructions. A program starts at address 300 (in decimal). Which one of the following is a legal program counter (all values in answers are in decimal)? Assume that each memory location is of one byte size. (2)

(a) 400 (b) 500 (c) 600 (d) 700

ii. Which one of the following is true for a CPU having a single interrupt request line and a single interrupt grant line? (1)

(a) Neither vectored interrupt nor multiple interrupting devices are possible
(b) Vectored interrupts are not possible but multiple interrupting devices are possible.
(c) Vectored interrupts and multiple interrupting devices are both possible
(d) Vectored interrupt is possible but multiple interrupting devices are not possible

iii. For the elements of sets {A,B,C,D} and {1,2,3,4} (1)

(A) DMA I/O	(1) High speed RAM
(B) Cache	(2) Disk
(C) Interrupt I/O	(3) Printer
(D) Condition code Register	(4) ALU

following is the correct matching:

(a) A-4 B-3 C-1 D-2 (b) A-2 B-1 C-3 D-4
(c) A-4 B-3 C-2 D-1 (d) A-2 B-3 C-4 D-1

iv. Purpose of start-bit in RS232C serial communication protocol is: (1)

(a) to synchronize receiver for receiving every byte
(b) to synchronize receiver for receiving a sequence of bytes
(c) a parity bit
(d) to synchronize receiver for receiving the last byte

v. In serial communication employing 8-data bits, a parity bit and 2 stop bits, the minimum baud rate required to sustain a transfer rate of 300 characters per seconds is: (1)

(a) 2400 baud (b) 19200 baud
(c) 4800 baud (d) 1200 baud

vi. A hard disk with a transfer rate of 10 Mbytes/second is constantly transferring data to memory using DMA. The processor runs at 600 MHz, and takes 300 and 900 clock cycles to initiate and complete DMA transfer respectively. If the size of the transfer is 20 Kbytes, what is the percentage of processor time consumed for the transfer operation? (3)

(A) 5.0% (B) 1.0% (c) 0.5% (D) 0.1%

vii. The following code is to run on a pipelined processor with one branch delay slot:

```
I1 : ADD R2 <- R7 + R8
I2 : SUB R4 <- R5 − R6
I3 : ADD R1 <- R2 + R3
I4 : STORE Memory [R4] <- R1
BRANCH to Label if R1 == 0
```

Which of the instructions I1, I2, I3 or I4 can legitimately occupy the delay slot without any other program modification? (2)

(a) I1 (b) I2 (c) I3 (d) I4

2. Suppose a stack representation supports, in addition to PUSH and POP, an operation REVERSE, which reverses the order of the elements on the stack.

(a) To implement a queue using the above stack implementation, show how to implement ENQUEUE using a single operation and DEQUEUE using a sequence of three operations. (3)

(b) The following postfix expression, containing single digit operands and arithmetic operators + and *, is evaluated using a stack. (3)

$$5\ 2\ *\ 3\ 4\ *\ 5\ 2\ *\ *\ +$$

show the contents of stack:

i after evaluation of 5 2 * 3 4 *

ii after evaluation of 5 2 * 3 4 * 5 2

iii at the end of evaluation.

3. Anew microprocessor is being designed with a conventional architecture employing single-address instructions and 8-bit words. Due to physical size constraints, only eight distinct 3-bit opcodes are allowed. The use of modifiers or the address field to extend the opcode is forbidden.

   (a) What eight instructions would you implement? specify the operations performed by each instruction as well as the location of its operands. (3)

   (b) Demonstrate that your instruction set is functionally complete in some reasonable sense; or if it is not, describe an operation cannot be programmed using your instruction set. (3)

4. It is required to design a hardwired controller to handle the fetch cycle of a single address of an instruction. The operand should be delivered in the fetch cycle itself. Assume that lower 8-bits of an instruction constitute the operand field.

   (a) Draw the logic schematic of the hardwired controller including the data paths. (4)

   (b) Give the micro-operations to realize the above instruction's fetch cycle. (3)

5. An instruction pipeline has five stages, each stage takes 2 nanoseconds and all instructions use all five stages. Branch instructions are not overlapped, i.e., the instruction after the branch is not fetched till the branch instruction is completed. Under ideal conditions,

   (a) calculate the average instruction execution time assuming that 20% of all instructions executed are branch instructions. Ignore the fact that some branch instructions are may be conditional. (3)

   (b) If a branch instruction is a conditional branch instruction, the branch need not be taken. If branch is not taken, the instruction following to that instruction can be overlapped. When 80% of all branch branch instructions are conditional branch instructions, and 50% of the conditional branch instructions are such that the branch is taken , calculate the average instruction execution time. (3)