30002:Computer Organization(Quiz#2 Solution)

November 12, 2013

Roll No. .....

Time: 25 minutes MM 10.

Instructions:

i. Open book quiz.

ii. All questions carry equal marks.

iii. Each correct answer carries 2 marks, and -1/2 mark for incorrect answer.

1. Consider a small two-way set-associative cache memory, consisting of four blocks. For choosing the block to be replaced, use the least recently used (LRU) scheme. The number of cache misses for the following sequence of block addresses: 8, 12, 0, 12,8 is,
(A) 2 (B) 3 (C) 4 (D) 5

Ans. 2 way 4 blocks, means total blocks are 4, and each block is 2-way. Thus total no. of sets are 2. The address fields are as shown below:

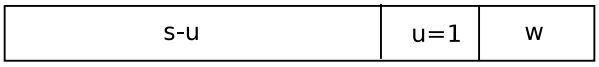

Figure 1: Question 1

The block addresses required to be used are: 8, 12, 0, 12, 0.
i. In the begin, the case is empty, so first block request for **8 is missed**. taking block address as $abcd^2$, the LSB bit d should indicate the set no. u, the position where block should be allocated. So set no is binary 0 or 1. In each set there are two positions, and the block will occupy the free position. For block address $8_{10} = 1000_2$, u is 0 so block will occupy 1st row in set 0, as follows:

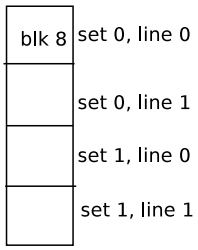

Figure 2: question 1, blk 8

ii. Block $12_{10} = 1100_2$, $u = 0$, so this block goes to set $u = 0$, at line 1. It is first time, so it is also **miss**.

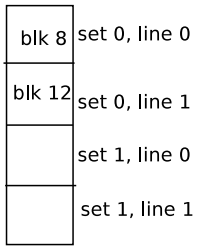

Figure 3: question 1, blk 12

iii. Block $0_{10} = 0000_2$, $u = 0$, so this block goes to set $u = 0$. Since there is no space at set set 0, so it replaces blk 8, as per LRU. It is first time, so it is also **miss**.

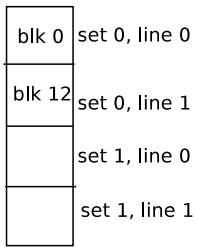

Figure 4: question 1, blk 0

iv. Block $12_{10} = 1100_2$, $u = 0$, so this block goes again to set $u = 0$. Since it already exists at line 1, it is **hit**.

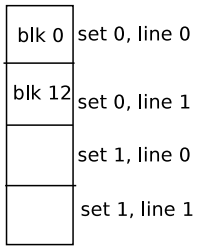

Figure 5: question 1, blk 12

v. Block $8_{10} = 1000_2$, $u = 0$, so this block goes again to set $u = 0$. Since it does not exists there, it is **miss**. It replaces block 8 there, as per LRU.

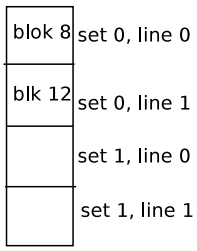

Figure 6: question 1, blk 8

Thus there are 4 misses, and 1 hit, so answer choice C is correct.

2. Consider a direct mapped cache of size 32 KB with block size 32 bytes. The CPU generates 32 bit addresses. The number of bits needed for cache indexing and the number of tag bits are respectively.
(A) 10, 17 (B) 10, 22 (C) 15, 17 (D) 5, 17

Ans. 32 bytes per block, $= 2^5$, $w = 5$,

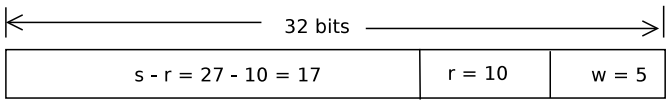

Figure 7: question 2.

cache size = 32 Kbyes = $32 \times 2^{10} = 2^5 \times 2^{10} = 2^{15}$, so lines in cache = $2^{15}/2^5 = 2^{10}$, so $r = 10$. $s = 32 - 5 = 27$. tag = $s - r = 27 - 10 = 17$. Since, index is r, $(r, tag) = 10, 17$. So, **answer is (A)**.

3. A CPU generates 32-bit addresses. The block size is 4 K Bytes. The processor has a Cache which can hold a total of 128 blocks and is 4-way set associative. The minimum size of the cache tag is:
   (A) 11 bits (B) 13 bits (C) 15 bits (D) 20 bits

Ans. block = 4K bytes = $4 \times 2_{10} = 2^{12}$. So $w = 12$. Cache size = 128 blocks = 2^7. 4-way set associative means, each set has 4 elements and the block corresponding to that block can fit any where in those. So, no. of set = $128/4 = 2^5$, so $u = 5$. total size of main memory in blocks = $2^{32-12} = 2^{20}$. So, $s = 20$. And tag = $s - u = 20 - 5 = 15$ Ans. is (C). see figure8

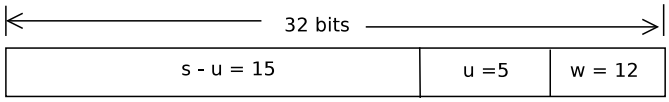

Figure 8: Question 3.

4. Consider a 4-way set associative cache consisting of 128 lines with a line size of 64 words. The CPU generates a 20-bit address of a word in main memory. The number of bits in the TAG, LINE and WORD fields are respectively:
   (A) 9, 6, 5 (B) 7, 7, 6 (C) 7, 5, 8 (D) 9, 5, 6

ans. Cache size = 128 lines = 2^7. Each set consists 4 blocks or lines. So, no. of sets = $2^u = 128/4 = 32 = 2^5$. Line size = block size = 64 words=2^6, so $w = 6$. Total no. of blocks = $2^{20}/2^6 = 2^{14}$, so, $s = 14$. see figure 9.

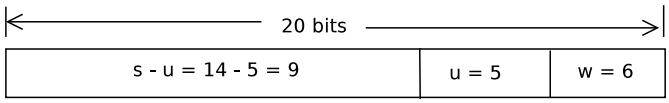

Figure 9: Question 4.

So TAG = 9, Line = 5 (The set no. decides the line. If, the line in the set no. u has tag field equal to corresponding bits in address, then it is hit), word = 6. So choice (D) is correct.

5. An 8KB direct mapped write-back cache is organized as multiple blocks, each of size 32-bytes. The processor generates 32-bit addresses. The cache controller maintains the tag information for each cache block comprises 1 Valid bit, 1 Modified bit, as many bits as the minimum needed to identify the memory block mapped in the cache. What is the total size of memory needed at the cache controller to store meta-data (tags) for the cache?
   (A) 4864 bits (B) 6144bits (C) 6656bits (D) 5376bits

Ans. 8 KB cache = $8 \times 2^{10} = 2^{13}$, block size = $32 = 2^5$, so $w = 5$. So, size of cache in no. of lines or blocks = $2^{13}/2^5 = 2^8$, so $r = 8$. blocks are $32 - w = 32 - 5 = 27$. So tag field = $32 - 8 - 5 = 19$ bits. total cache size 2^8 rows. Total bits in cache control memory are 19+1+1 = 21. So in 2^8 locations of cache, total bits are $2^8 \times 21 = 5373$ bits. So answer is D. See figure 10.

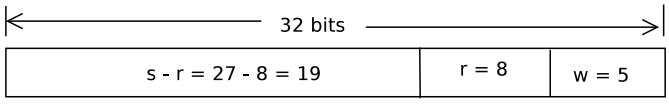

Figure 10: Question 5.