30002:Computer Organization(Quiz#2)

November 7, 2013

Roll No. .....

Time: 25 minutes MM 10.

Instructions:

i. Open book quiz.

ii. All questions carry equal marks.

iii. Each correct answer carries 2 marks, and -1/2 mark for incorrect answer.

1. Consider a small two-way set-associative cache memory, consisting of four blocks. For choosing the block to be replaced, use the least recently used (LRU) scheme. The number of cache misses for the following sequence of block addresses: 8, 12, 0, 12,8 is,
   (A) 2 (B) 3 (C) 4 (D) 5

2. Consider a direct mapped cache of size 32 KB with block size 32 bytes. The CPU generates 32 bit addresses. The number of bits needed for cache indexing and the number of tag bits are respectively.
   (A) 10, 17 (B) 10, 22 (C) 15, 17 (D) 5, 17

3. A CPU generates 32-bit addresses. The block size is 4 K Bytes. The processor has a Cache which can hold a total of 128 blocks and is 4-way set associative. The minimum size of the cache tag is:
   (A) 11 bits (B) 13 bits (C) 15 bits (D) 20 bits

4. Consider a 4-way set associative cache consisting of 128 lines with a line size of 64 words. The CPU generates a 20-bit address of a word in main memory. The number of bits in the TAG, LINE and WORD fields are respectively:
   (A) 9, 6, 5 (B) 7, 7, 6 (C) 7, 5, 8 (D) 9, 5, 6

5. An 8KB direct mapped write-back cache is organized as multiple blocks, each of size 32-bytes. The processor generates 32-bit addresses. The cache controller maintains the tag information for each cache block comprises 1 Valid bit, 1 Modified bit, as many bits as the minimum needed to identify the memory block mapped in the cache. What is the total size of memory needed at the cache controller to store meta-data (tags) for the cache?
   (A) 4864 bits (B) 6144bits (C) 6656bits (D) 5376bits