IIT Jodhpur, II Mid Sem. Examination
Computer Science & Engineering V Sem. 2014
30002:Computer Organization

Max. Marks=30 Time= 1 Hr.

1. Consider a processor in which each instruction is 16-bit size. The following contents appears in main memory, starting at location 200. Each memory location holds one byte.

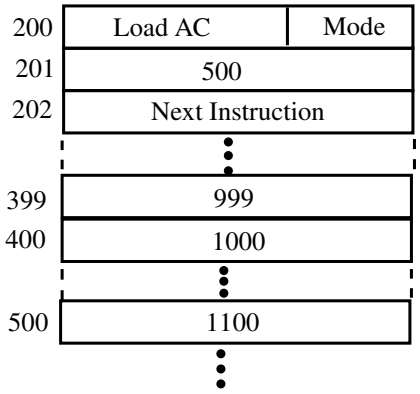

Figure 1: Three locations of main memory.

The first part of the first instruction indicates that this instruction loads a value into an accumulator. The *mode* field specifies addressing mode and, if appropriate a *source register* (depending on the addressing mode used). Assume that when used, the source register is R_1 having a value inside of 400. There is also a *base register* that contains the value 100. The value 500 in location 201 may be part of the address calculation for some instructions. Determine: (1) effective address and (2) value of operand to be loaded into accumulator for the "*Load AC*, ..." instruction when following addressing modes are used: (6)

(a) Direct
(b) Indirect
(c) Immediate
(d) Displacement
(e) Register
(f) Register Indirect

2. There is a variable-length opcode to allow all of the following to be encoded in a 32-bit instruction, with each memory location of one byte size, and total eight general purpose CPU registers. Suggest a suitable instruction set architecture, addressing modes, and types of instructions: arithmetics, logical, and control instructions, like conditional and unconditional jumps and subroutine calls. (6)

- Instructions category 1, have three operands: two 13-bit addresses and one 3-bit register number.
- instructions category 2, have two operands: one 13-bit address and one 3-bit register number
- Instructions category 3, with no address or registers (i.e., implied address)

3. Write a PDP-8 Assembly language program to sum an array of 16 elements, and store the result at location 0357_8. Each element is 12-bit length and occupies single memory location. The "program" and "data" of array are stored in page number one of the memory as shown in figure 2. (5)

The size of instructions is fixed 12-bits ($D_0 - D_{11}$), with bit D_0 as MSB and bit D_{11} as LSB, the bits are used as follows:

bits $D_0 - D_2$ are 3-bit opcode,

bit $D_3 = 0$ means direct address, and $D_3 = 1$ means indirect address.

bit $D_4 = 0$ means zero page, and $D_4 = 1$ means current page (in which instruction is)

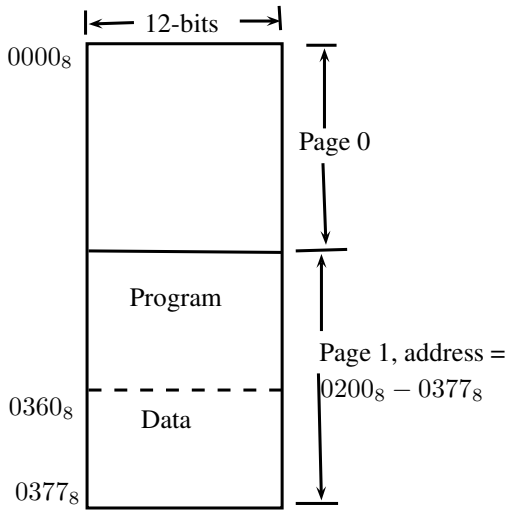

Figure 2: Memory with program and data.

bits $D_5 - D_{11}$ is 7-bit offset for data address (other bits are taken as zeros to form the address)

(a) What should be the values of bits D_3, D_4 to access the data?

(b) Should the program use direct or indirect addressing mode?

(c) Where would you maintain the "data pointer" and "counter"?

(d) Should we up-count or down-count? Justify.

(e) Explain the logic of steps of above assembly language program.

(1, 1, 2, 1, 3)

4. By analyzing the program below, write the expression that is computed using the stack architecture. Assume A, B, C, D, E, F, G, H are the register names to hold values a, b, c, d, e, f, g, h, respectively. (5)

```
PUSH B
PUSH C
PUSH D
MUL
PUSH E
MUL
PUSH F
PUSH G
MUL
PUSH H
ADD
SUB
ADD
POP A
```