Indian Institute of Technology Jodhpur

Computer Organization (CS30002) End Semester Examination

July-November, 2014 *Duration 3 Hours* *Date-24/11/2014*

Instructions:

- This question paper is in two pages.
- Read the questions carefully.
- Avoid seeking clarifications from the invigilators, unless it is very necessary.
- All questions are complete in every respect.
- Attempt all questions.

---

1. (a) Given RAM memory chips of 16 k X 8-bits each, how you will construct a 64 k X 8-bit memory system. The CPU has $A_0 \ldots A_{15}$ address lines, and 8 data lines. Each memory chip has $A_0 \ldots A_{13}$ address lines, 8-data lines, and a chip select line. Draw the the inter-connections for the memory system. [4]

   (b) Consider a 32-bit RISC micro-processor with 32-bit data-bus and 32-bit address bus. The CPU operates at 1 GHz clock rate, and memory *load* and *store* instructions each take two CPU clock cycles. Memory-mapped IO is used and CPU supports both vectored and non-vectored interrupts, and DMA block-transfer with arbitrary block length. Typical interrupt response time is 10 CPU clock cycles. It is desired to add to the system, a disk drive with a data transfer rate of N-bits /sec. Estimate the maximum value that N can have for each of the following ways of controlling disk drive: [3+3]

      i. Programmed IO using interrupts

      ii. DMA

   Show all you calculations and state the assumptions you have made for both hardware and software.

2. (a) Consider a cache with a line size of 64 bytes. Assume that on average 30% of the lines in the cache are dirty (modified). A word consists of 8 bytes. Assume there is a 0.97 hit ratio. Compute the amount of main memory traffic, in terms of bytes per instruction for both *write-through* and *write-back* policies. Memory is read into cache one block at a time, with block size equal to line size. However, for write back, a single word can be written from cache to main memory. [4]

   (b) Design a cache memory system with 8-way 4 MB set associative cache memory, with line size and block size of 32-bytes. The size of main memory is 2 GB. Answer the following for this cache: [2+1+1+2]

      i. How address mapping is done for a block in RAM with the line in cache?

      ii. What are the sizes of: Tag field, offset, and set ?

      iii. What is effect of increasing and decreasing the number of sets?

      iv. What block replacement algorithms you would use for following? justify.

         A. banking transactions (same algorithm for most transactions)

         B. university computing (different algorithms)

3. (a) Consider that in a CPU there are 8-interrupts, $I_0 \ldots I_7$. Design an interrupt priority system, such that I_j has higher priority than I_i, when $j > i$. There can be any number of interrupts active at a time but CPU will serve the highest priority. [4]

   (b) An IO processor (IOP) controls the data transfer between main memory and set of IO devices with widely varying data transfer rates. The IOP can interleave (multiplex) transfers involving several IO devices provided that their combined effect does not exceed data transfer capacity of the system. The Data transfers are initiated by requests from the IO devices. A request is accepted by IOP only if it has sufficient spare capacity to service the requesting IO device. Write an algorithm to be run by the IOP to determine whether or not it can service a request from the next IO device. [6]

4. (a) Consider matrix multiplication operation on two matrices $A[4, 5]$ and $B[5, 6]$, producing a result matrix $C[4, 6]$. The matrices are stored in RAM in row major order (each row is stored in consecutive memory locations). Design a pipeline to compute the resultant matrix. Answer the following: [2+2+2]

      i. How many pipeline segments you suggest ? Justify.

      ii. What is instruction format and why?

      iii. How the resultant matrix is computed?

   (b) A hypothetical time-sharing system has following properties. The system handles up to four concurrent jobs ($p_1 \ldots p_4$), each requiring on the average of 5 secs of CPU time, which is allocated to the job in the time-slice manner with each slice of 50 msec. The CPU processes a job until an IO operation is required or time slice is over. The IO operation is *page swap* with secondary memory, and requires 100 msec. Find out the following performance measures: [2+2]

      i. Mean response time (time to complete a job) when there are four active jobs.

      ii. The mean fraction of time the CPU is idle.

Following does not carry any marks and optional for attempting:

5. Rewrite these topics in preferential order of your liking (the best as first:)

Assembly language, RISC/CISC, interrupts/DMA, control design, Micro-programmed control, arithmetics, gate logic and flip-flops, cache, IO devices, Parallel computing.

BEST WISHES !!