Computer Organization' 2014
Exercises sheet # 1

1. Construct a SR Flip-flop using NAND gates only.
2. Construct a D Flip-flop using NOR gates only.
3. Construct a 4-bit decade counter using appropriate components.
4. Find a minimum cost implementation of the function $f(x_1, x_2, x_3, x_4)$, where $f = 1$ if either one or two of the input variables have the logic value 1. Otherwise, $f = 0$.
5. Prove that associative rule does not apply to the $NAND$ operator.
6. How you will construct a down counter, i.e, from 1111 to 0000 ?
7. The address lines $A_0 \ldots A_{15}$, use encoder to access the corresponding physical address (T/F).
8. What is the Boolean expression for the output o for multiplexer shown in figure 1?

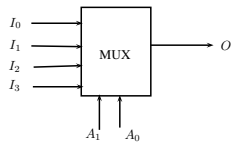

Figure 1: 4-Input multiplexer.

9. Consider the circuit shown in figure 2 involving positive edge trigged D-FF, as well the corresponding timing diagram. Let A_i represents the logic level on the line A in the i^{th} clock period.

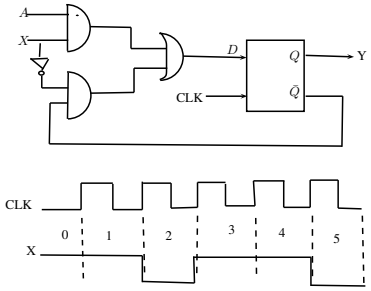

Figure 2: D-FF circuit

Let A' represents the complement of A. The correct output sequence Y over the clock period 1 through 5 is:
A) $A_0A_1A_1'A_3A_4$ B) $A_1A_2A_2'A_3A_4$
C) $A_0A_1A_2\prime A_3A_4$ D) $A_1A_2'A_3A_4A_5$

10. Consider the circuit composed of XOR gates (figure 3) and non-inverting buffers. The non-inverting buffers have delays of $\delta_1 = 2ns$ and $\delta_2 = 4ns$. Both XOR and wires have zero delays. If the above waveform's 7-cycles are applied at input A, how many transition(s) (change of levels) occur at B during the interval $0 - 7ns$?

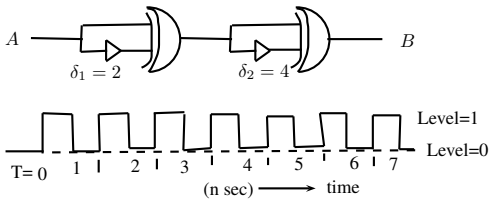

Figure 3: XOR Circuit and waveform.

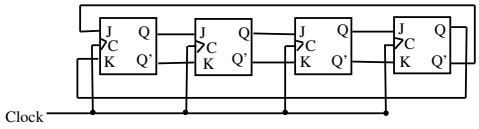

Figure 4: JK Flip-Flops.

11. Investigate the operation of circuit in fig. 4). Assume an initial state of 0000(=output of four flip-flops). Trace the output (the Qs) as the clock ticks and determine the purpose of the circuit.

Note: submission deadline: Online in word/pdf: 02/09/14 11.59 PM) at kr.chowdhay[at]iitj.ac.in, mark subject as roll no.