Computer Organization' 2014
Exercises sheet # 2

1. Determine the maximum speedup of a single-bus multiprocessor system having N processors if each processor uses the bus for a fraction f of every cycle.

2. When Bus Adapters are used for generating more buses, we can also have one such bus exclusively for memory sub-systems, one fast bus and a slow bus for appropriate types of I/O devices. Sketch such an arrangement and discuss the modes of data transfer between the main processor-memory bus and each of these different backplane buses. Also outline how communication may be established between units across the different backplane buses.

3. Develop the asynchronous interlocked two-way communication protocol between a handshaking master and a slave involved in a write cycle, and sketch the relevant timing waveforms.

4. Assuming appropriate handshake signals, indicate the series of actions involved in priority arbitration sequence, and show how they mesh in with the on-going parallel action of data transfer.

5. A computer has 64-bit instructions, having two fields: first two bytes are for opcode, and the rest is immediate operand or operand address.

   (a) What is maximum addressable memory in bytes?

   (b) How many bits are required for program counter and for IR?

6. A computer has 16-bit address and 16-bit data-lines.

   (a) What is maximum address space?

   (b) What is size of each location in bytes?

   (c) What is size of PC, AR, DR, IR?

7. Two microprocessors have 16- and 32-bit wide external data buses. Other features are same and bus cycles are identical.

   (a) If all instructions and operands are 4 bytes long, by what factor the maximum data transfer rate differ?

   (b) Repeat above, if half of the instructions and opcodes are two-bytes long.

8. For the synchronous read operation, the memory module must place the data on the bus sufficiently ahead of the falling edge of the Read signal to allow for the signal settling. The clock frequency is 20 MHz and Read signal begins to fall in the middle of the second half of T_3.

   (a) Determine the length of the memory read cycle.

   (b) When, at the latest, should memory data be placed on the bus? Allow 10 ns for settling of data lines.

9. Intel 8088 microprocessor has read bus timing like the synchronous read/write discussed in the class, but it requires 4 clock cycles. The valid data is on the bus for an amount of time that extends into the 4th cycle. Let clock is 8 Mhz.

   (a) What is the maximum data transfer rate?

   (b) Repeat above, assume the need to insert one wait state per byte transferred.

10. 8086 uses 16-bit bus that can transfer 2 bytes at a time, provided that lower byte has even address. However, the 8086 allows both even- and odd-aligned word operands. If odd aligned word is referenced, two memory cycles, each consisting of four bus cycles, are required to transfer the word. Consider an instruction on 8086 that involves two 16-bit operands. How long does it take to fetch the operands? Give range of possible answers. The clock is 4 Mhz and no wait state is present.

Submission deadline: 24 Sept. 11.59PM. preferable online. Offline: as hard-copy using A4-plain sheets stapled together on 25th.