

Time 1 Hr.

Max. Marks=20.

Instructions:

- i Write the complete method/procedure/justification, where required, merely writing the answers is not sufficient.
 - ii Rough work should be done at the end of answer sheet. Any thing which is not part of answer must be deleted.
1. If the operands are in 2's complement representation, what operations out of A+B, A-B, A++, B++ (increment by 1) can be performed using the ALU diagram shown in figure 1? (6)

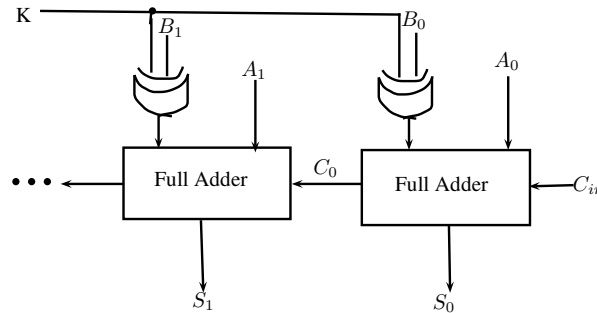


Figure 1: ALU

Ans. With $k = 0, c_{in} = 0$, input to full adders is $\dots A_1 A_0$ and $\dots B_1 B_0$. This produces addition, with carry propagated to each next full adder.

With $k = 1$ and $c_{in} = 1$, EX-or complements the B s and $c_{in} = 1$ produces its 2's complement effectively, that when added with A s produces the $A - B$.

With $\dots A_1 A_0 = \dots 00, k = 0, c_{in} = 1$, produces $B ++$.

With $\dots B_1 B_0 = \dots 00, k = 0, c_{in} = 1$, produces $A ++$.

2. Find the maximum clock frequency at which the counter shown in figure 5 can be operated. Assume that the propagation delay through each flip-flop and AND gate combined is 10 nsec. Also assume that setup time (time to stabilize signal) for the JK flip-flop inputs is negligible. (6)

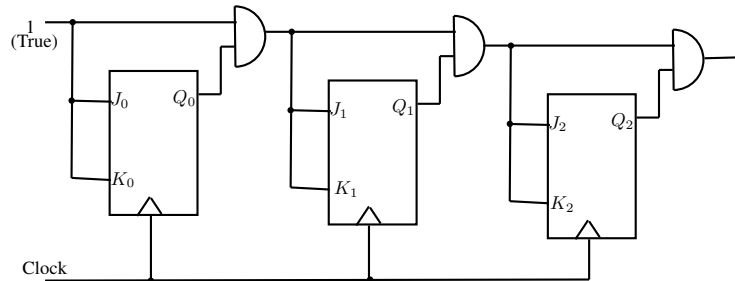


Figure 2: Counter

Ans. With $jk = 11$, the JK FF toggles. Therefore, the Q_0 FF always toggles, on every rising edge of clock. Thus output of Q_0 frequency is just half of clock input. FF1+D FF propagation delay is 10 ns. Hence the max frequency is 100 MHz ideally. The waveforms are given below.

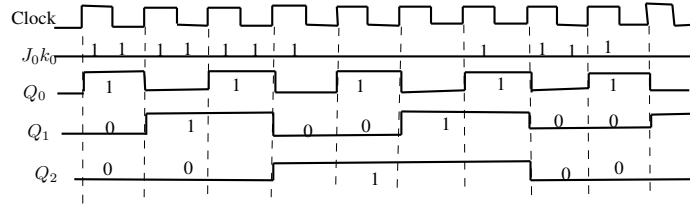


Figure 3: Counter wave-forms

J_1k_1 follows Q_0 always with a propagation delay equal to of NAD gate. Q_1 toggles when $J_1k_1 = 11$ on arrival of clock pulse. J_2k_2 follows Q_1 , and Q_2 toggles when $J_2k_2 = 11$.

Clock should not arrive when propagation is in progress, (10 ns), so clock freq = 100 Mhz.

- Consider that a line printer (a high speed printer) is connected through bus using a IOP (IO processor). The other components connected to this bus are CPU and memory. Assume that printer operates in asynchronous mode using hand-shake signals. Every time the printer requires the data (from memory), IO processor requests bus control so that it (IOP) can read 132 bytes in 132 clock cycles from the memory. Having received these many bytes, the read operation by IOP is over. Assume that after printing of these 132 chars (bytes) by printer, which takes 50 milli-sec, the IOP again requests the bus for data transfer of one line (i.e., 132 chars) and it goes on (in case of a large file to be printed). Assume that processor clock speed is 100 MHz.

Draw the necessary waveforms, indicating clock, data, handshake signals, using which explain the communication between memory, IOP, CPU. Assume that CPU is bus master. (8)

Ans. For 100 MHz, 1 clock = 10 ns. no. of clocks in 50 msec. = 5×10^6 . The figures below show the connections of interfacing and waveforms.

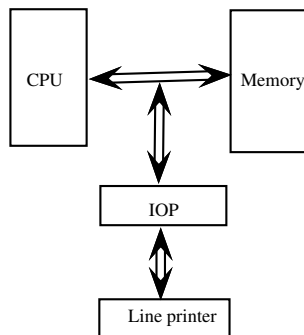


Figure 4: Bus Interface with IOP and printer.

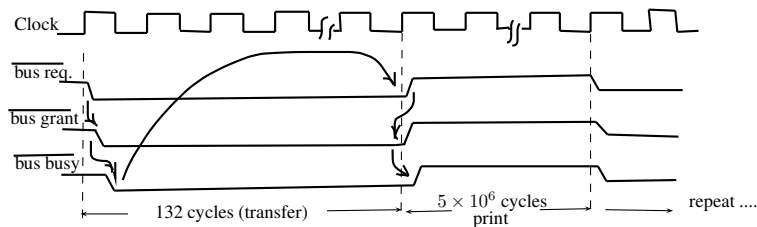


Figure 5: Data transfer and printing with printer.