2nd Mid Semester Examination
Computer Science & Engineering I Sem. 2013-14
30002: Computer Organization

Time 1 Hr. Max. Marks=15.

Instructions:

(i) Write the complete method/procedure, where required, merely writing the answers is not sufficient.

(ii) The rough work should be done at the end of booklet. Any thing which is not part of answer must be deleted.

1. A magnetic storage disk has following parameters: there are 20 data recording surfaces, with 15,000 tracks per surface. There is average 400 sectors per track and each sector contains 512 bytes of data. Data is stored in units of blocks, with block size 8k bytes. The average seek time of disk is 6 msec. The disk rotates at 10,000 revolutions per minute. The average data transfer rate from a track to data buffer in disk controller is 34 M bytes/sec. When connected to system bus, a drive of this type can have maximum data transfer rate of 160 M bytes /sec.

Ans. The average seek time and rotational delay are 6 and 3 ms, respectively. This is because, 10,000 rpm = 10,000/60 rps. One rotation time = 60/10,000 sec. and, Half rotation time = latency time = 3 ms. The average data transfer rate from a track to the data buffer in the disk controller is 34 Mbytes/s. Hence, it takes 8K/34M = 0.23 ms to transfer a block of data. Note: Out of bus transfer rate v/s disk controller transfer rate, the lower one will be valid for transfer with disk.

(a) Assume that blocks required for a file are randomly placed in the disk, what percentage of the total block transfer time is consumed by seek operations and rotational delays(latency) put together. (2.5)

Ans (a) The total time needed to access each block is seek + latency time + block transfer time = 6 +3 + 0.23 = 9.23 ms. The portion of time occupied by seek and rotational delay is 9/9.23 = 0.97 = **97%**.

(b) Assume that disk accesses have been arranged so that in 90 percent of the cases, the next access will be to a data block on the same track. What percentage of the total block transfer time is consumed by seek operations and rotational delays(latency) put together. (2.5)

Ans (b) For 90% cases, the seek time is nil, because the next access is on same data block. So total seek time = $0.1 * 6 = 0.6$. The latency time depends on rotational speed, hence unaffected by this. So total latency time = 3. Therefore, the average time to access a block is $0.6 + 3 + 0.23 =$ 3.83 ms. The portion of time occupied by seek and rotational delay is 3.6/3.83 = 0.94 = **94%**.

2. Analyze the following 8085 code, explain its function, and write an equivalent algorithm for the same. (5)

```
PROGRAM:
      MVI D, 00
      MVI A, 00
      LXI H, 4050
      MOV B, M
      INX H
      MOV C, M
LOOP: ADD B
      JNC NEXT
      INR D
NEXT: DCR C
      JNZ LOOP
      STA 4052
```

```
MOV A, D
STA 4053
HLT
```

Ans. Consider that memory location 4050 has its content as x and 4051 has its contents as y. The program decrements y and each time x is added into accumulator, until y becomes 0.

Thus effectively, $\mathbf{x} * \mathbf{y}$ has been put into accumulator. Since, multiplication result may be larger than what accumulator can hold, hence, every time carry is generated due to addition, the register D is incremented by 1. Thus, effectively, The register set DA holds the result $x * y$, with higher byte in D. The lower and higher bytes are stored at memory locations 4052 and 4053, respectively.

```
 %algorithm
 x = byte; x at 4050
 y = byte; y at 4051
 A <- 0
 D <- 0
 C <- y
while c > 0 do
   A <- A + x
   if carry then D <- D +1
   C <- C -1
endwhile
x <- A
y <- D
stop
```

3. (a) write an assembly language program for R-R architecture machine, for the following expression,

$$S = \sum_{i=0}^{i=n-1} a_i$$

where, a_i are array elements at consecutive memory locations. Write the micro-operation codes for each of the above assembly instructions. (2.5)

Ans.
```
; R0 as accumulator
; R1 as counter
; R2 as memory pointer
; R3 as temporary register
      LOAD R0, #0
      LOAD R1, #n ; value of n is loaded
      LOAD R2, #addr of a0
loop: LOAD R3, (R2) ; get data
      ADD R0, R3
      ADD R2, #1 ; advance memory pointer
      SUB R1, #1 ; decrement counter
      BNE R1, #0 ; branch on R1 not equal to zero
      STOR R0, S ; store sum at S
      HLT
```

(b) The RAM memory of size M locations requires M drivers for single dimensional memory. If the RAM is organized as 2-D, and there are m row and n columns, such that $m \times n = M$, with total $m + n$ drivers, and $M > (m + n)$. Show that number of drivers are minimum if and only if $m = n$. (2.5)

Ans. Considering M = 16 as total memory size, the value of rows(m) and columns (n), the table can be given as:

m	n	$M = m * n$	total drivers $d = m + n$
1	16	16	17
2	8	16	10
4	4	16	8
8	2	16	10
16	1	16	17

We note that total number of drivers $m + n$ are minimum when they are equal (each 4). Considering m and n as sides of a rectangle, for given area. We note that for that area, $m + n$ is minimum when $m = n$. This can also be proved for minimization, by taking derivative for minimization/maximization.