Computer Science & Engineering, V Sem. 2014-15(1st Mid. Sem)

30002: Computer Organization

Time 1 Hr. Max. Marks=20.

Instructions:

i Write the complete method/procedure/justification, where required, merely writing the answers is not sufficient.

ii Rough work should be done at the end of answer sheet. Any thing which is not part of answer must be deleted.

1. (a) Write the decimal number 86.5625 as a normalized binary number in scientific notation (i.e., in $0.xxxx...2^{xx...}$ format, where x's are 0's and 1's). (2)

   Ans. $0.10101101001 \times 2^{111}$.

   (b) Write the number in (a) in IEEE single precision floating point format. Give your answer in hexadecimal. (3)

   Ans. Total length is 32 bits (1 bit sign, 8-bits biased exponents, 23-bits mantissa). The number is 1.0101101001×2^6. So exponent in biased form is $6 + 127 = 133$. This is binary 10000101. So the IEEE 754 format value is:

$$
\begin{aligned}
&= 0\ 10000101\ 01011010010000000000000 \\
&= 0100\ 0010\ 1010\ 1101\ 0010\ 0000\ 0000\ 0000 \\
&= 42AD2000
\end{aligned}
$$

2. Given there is a Comparator block in figure 1 with two inputs words A and B each of two bits. The comparator gives output z as binary 0 if both words are equal and 1 if they are unequal. Use any suitable method to design a minimized logic circuit representing the comparator block. (5)

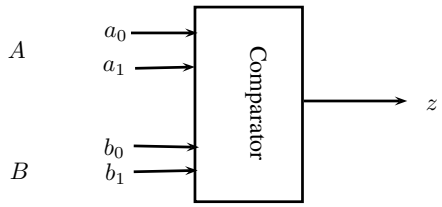

Figure 1: 2-bit words comparator.

Ans. The implementation of comparator, with output expression $z = (a_0 \oplus b_0) + (a_1 \oplus b_1)$ is shown in figure 2.

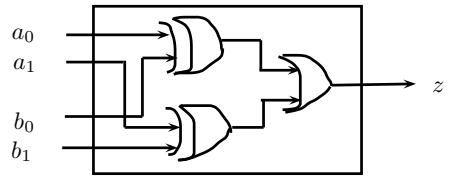

Figure 2: 2-bit words comparator logic.

3. Make use of four T-flip-flops to construct a decade counter. That is, it may have any initial value $(0000_2 - 1001_2)$ at the True output Q_3, Q_2, Q_1, Q_0. When started, it will up count and reset the counters and restart counting from 0000_2 when the output has reached to 1001_2. (5)

Ans. The decade counter is shown in figure 3. It resets when output becomes 1010.

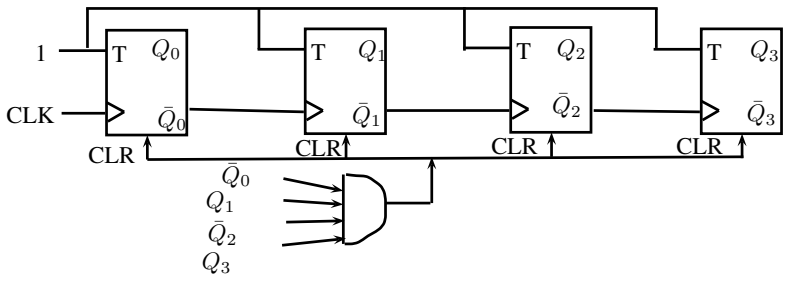

Figure 3: Decade counter.

4. Make use of logic gates and flip-flops, to design an automatic door opener. The door "open" or "close" operations are done by sending the '1' or '0' at the output y, respectively. The "open" and 'close" commands are given by pressing two buttons, as shown in figure 4. When the "open" button is pressed and released, it sets the output to true. Similarly, when "close" button is pressed and released it resets the output to 0. If both the buttons are pressed together, the state remains un-changed. Design and describe the logic circuit inside the box of this figure. (5)

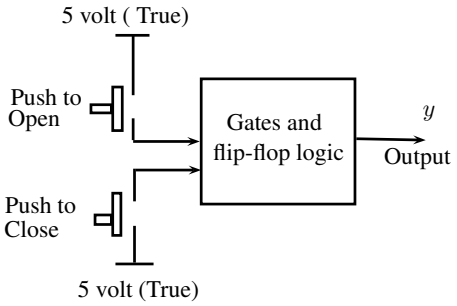

Figure 4: Automatic door opener.

Ans. Let $a = 1$ is for open, and $b = 1$ is for closed. Both these are true when push buttons are pressed. The table for the logic is given as table 1 and K-map is shown in figure 5.

Table 1: Door operation table.

a	b	Output $z(q_{i+1})$
1	1	q_i (unchanged)
1	0	1 (open)
0	1	0 (closed)
0	0	$q_i$unchanged

As per figure 5, we get next state of door based on the button pressed as:

$$q_{i+1} = a\bar{b} + aq_i + \bar{b}q_i$$

The logic diagram of this is given in figure 6.

There are more than one solutions for this problem. These are shown in figure 7.

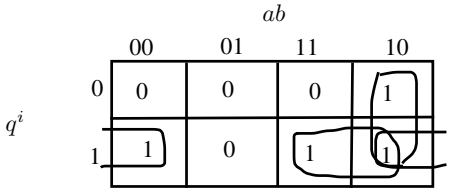

Figure 5: Automatic door opener K-map.

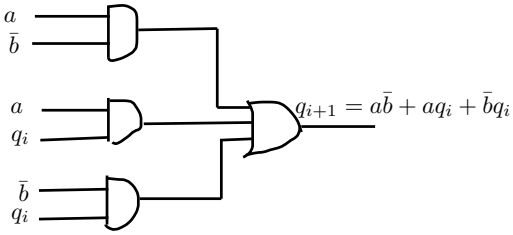

Figure 6: Automatic door opener K-map logic.

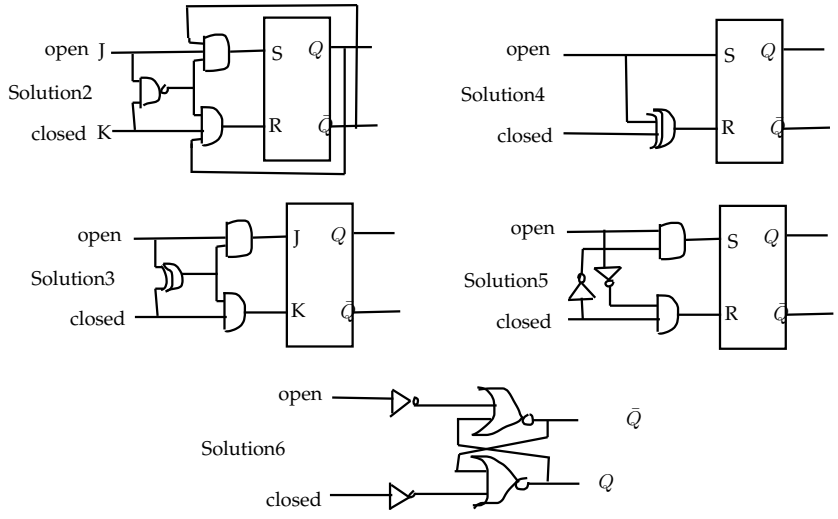

Figure 7: Automatic door opener K-map logic.