



Systems Society of India

9<sup>th</sup>

**National  
Systems  
Conference**

**PROCEEDINGS**

NSC—85

21-23 December, 1985



Motilal Nehru Regional Engineering College  
Allahabad India

MICROPROCESSOR BASED DATA ACQUISITION SYSTEM  
FOR ATOMIC POWER PLANTS

K.R. Chowdhary\*

Summary

This paper presents a scheme to monitor the status of fuel rod elements in a nuclear Reactor Plant, for detection and identification of fuel failure. A Microprocessor-based system was developed and used for this purpose, to replace an obsolete system which used hardwired logic. The fault tolerance and reliability of the new system is also discussed.

Introduction

In a nuclear reactor it is very important to detect any fuel failure at the earliest stage. Any delay in detection or corrective action will spread the contamination and activity in all the areas where primary coolant pipings are routed. A minor pinhole formation or a crack in the fuel cladding which houses the fuel is termed as a "fuel failure" or "split rod". Such a pin-hole or crack will allow the radioactive nuclides to find their path through and mix with the coolant medium. The requirement is to locate the correct failed fuel position by a suitable monitoring method so that timely action can be taken to shut-down the system before the radio-activity spreads out. Using one detector for monitoring the activity of each fuel rod is one of the possible methods of monitoring the fuel failure, but this method is highly cost ineffective due to the requirement of large number of detecting elements (approximately 200 numbers).

A better approach is to use a matrix method in which the coolant outlet from each fuel rod is monitored by two different detectors, each one monitoring bulk mixer of coolant outlet from many fuel rods. If there is split in any fuel rod, the two corresponding detectors which monitor its coolant outlet will give higher signals. In

this way each fuel rod position signifies a unique pair of detectors. The minimum number of detectors required for this system should be such that the number of possible combinations of unique pairs are equal to the total number of fuel rods, so that failure in any of the fuel rods can be identified by its designated unique pair of detectors indicating high signal levels. Suppose N number of detectors are used for this system, then possible combination of unique pairs are -

$$N(N-1)/2 = F \text{ (Total number of fuel rods)}$$

For a given number of fuel rods F, the number of detectors required (N) is rounded up to the next higher integer value. In this way a reactor\*\* of 190 fuel elements can be monitored with a total of only 20 detector elements as against to 190, when one detector per fuel rod is used. Since there are, total 380 outlet sample connections for 190 number of fuel rods, each detector will monitor affluent coolant water from 19 fuel elements.

A hardwired monitoring and annunciation system, based on relay logic, was in operation for a long time. For an application like monitoring of nuclear-reactor fuel in-pile, the need of reliable information cannot be over emphasised. At the same time the monitoring system must have the MTBF (Mean Time Between Failure) as high as possible. For detection of malfunctioning or failure of the instrument itself a micro-processor or computer-based system is most suitable and seems to be the only solution.

---

\* The author is Associate Professor with the Department of Electronics and Commn Engg, University of Jodhpur, Jodhpur. Before this he was with B.A.R.C. as Senior Scientific Officer.

## Microprocessor-based System

### (a) Hardware:

A micro-based system, using 8085 Processor was designed and installed for monitoring-cum-annunciation. The 8085 Microprocessor suited better for applications like--industrial control and data acquisition, for it has large number of CPU registers with sufficient number of maskable interrupt lines--a criteria for online applications. Another reason, for selection of 8085 has been that all the support chips of intel 8085 processor were easily available in the Indian Market.

In the hardware configuration (Fig.1) it uses 4 K bytes of ROM, 1.25 K bytes of RAM, one 14 bit timer, I/O ports, one 8 bit Analog to Digital Converter and two 8 bit Digital to Analog convertors.

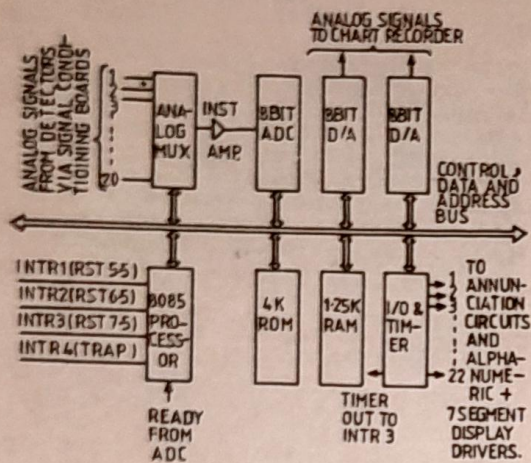


Figure 1. System Configuration.

The analog signals from detectors are suitably conditioned before they reach to the microprocessor board. Zener limiters were used in the input circuitry to constrain signals against abnormal rise in amplitude due to any malfunctioning in the incoming

circuitry. Frequency response is kept from DC to 34 Hz to reject 50 Hz mains disturbance and the frequencies above this. Due to hydraulics of the physical system being monitored, the actual frequency response of interest lies below 10 Hz only.

For the purpose of saving an interrupt, Analog-to-digital conversion is controlled by utilising the READY line and creating a wait state to stretch the execution cycle of 8085. During the period of analog channel selection by multiplexer and A to D conversion, processor remains in the WAIT state for about 150 micro-seconds. It is understood that this reduction in processing speed due to longer time for A to D conversion has no effect on the performance of the system due to the fact that the system being monitored is a process of low frequency response and slow in nature. Two D/A converter output signals represent the boundaries (maximum and minimum), out of 20 detector signals being monitored, and recorded on a process chart recorder. The 4 K byte ROM accommodates 1 K monitor which operates on RS-232-C serial interface; and 3 K bytes of operating system program. 1.25 K bytes RAM is required for storing the scanned input data, stack, status of the ports and their command words, counters, and diagnostic data. I/O ports drive the alarm annunciation circuits and alphanumeric display buffers while the 14 bit timer is used for timely maintenance of scheduling, of all the real-time activities in the system including the system diagnostics.

### (b) Software:

Software (Fig.2) for this system was written in 8085 assembly language (1) and developed on a cross assembler available on Prime 450 Computer System at BARC. Complete software is divided into four different utilities, each one sub-divided into many different tasks. A 1 K byte resident serial monitor was found to be very helpful tool for debugging at the final stage of programme development. This was achieved by keeping the operating system in a E<sup>2</sup> PROM and modifying it on-line whenever the change was needed, using a Burroughs micro-terminal. Once the software was finalised, the monitor program was kept resident

\*\* This system was designed for CIRUS Reactor, B.A.R.C., which houses 190 number of fuel elements.

permanently within the system for future modifiability and upgradability of the operating system and alteration of alarm set point values for the process parameters, which remain in an E<sup>2</sup> PROM.

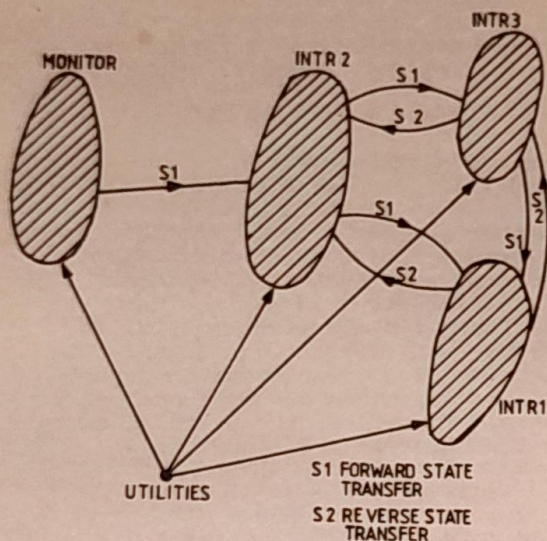


Figure 2. Software utilities.

Depression of an 'operate' key on the console generates RST 6.5 interrupt and the control is transferred to the main utility (Fig.3a) of the operating system. This routine keeps looping at a rate of 3.623 times per second so as to match the requirement of frequency response characteristics of the physical system being monitored. Provision is made to evoke RST 5.5 interrupt manually from the control panel. This will produce a simultaneous scan of channel number against its latest input signal magnitude sequentially on panel displays, at a rate so that it can be easily noted down or the relative signal strength of the input channels can be compared. Latest magnitude of input signal remains stored in the memory data buffer. At the end of display scan, processor returns back to the original utility.

RST 7.5 utility is evoked by the termination count of a 14 bit timer of 2.666 milli-seconds duration and this is repeated after every 2.816 milli-seconds. This utility (Fig.3b) is incorporated to achieve the following:

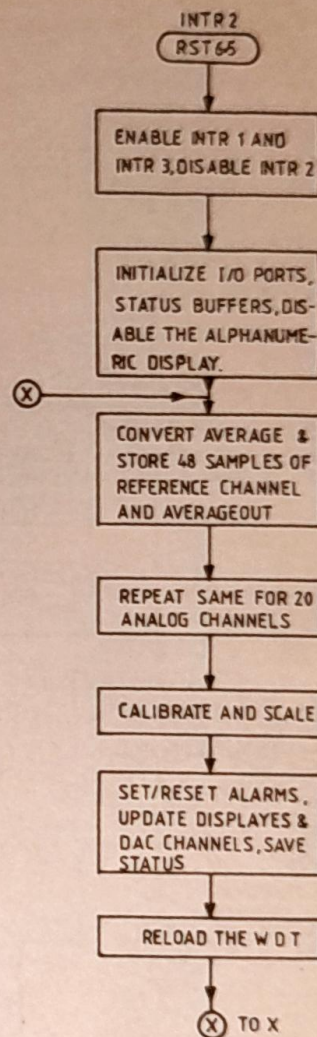


Figure 3(a). Data acquisition routine

(1) Each cycle of RST 6.5 utility is interrupted many times by RST 7.5 interrupt. The latter every time decrements a WDT (Watch-dog-timer) count by unity while causing interrupt. At the end of its execution RST 6.5 utility always restores the WDT count which otherwise is made to underflow by RST 7.5. WDT underflow is indication for system malfunctioning due to either software or hardware failures and consequently main program routine is not properly executed. In such circumstances RST 7.5 routine initialise the system

again and execution starts from the beginning of main program. If second time again the WDT underflows, a flag is raised for indication and control gets transferred to the manual mode.

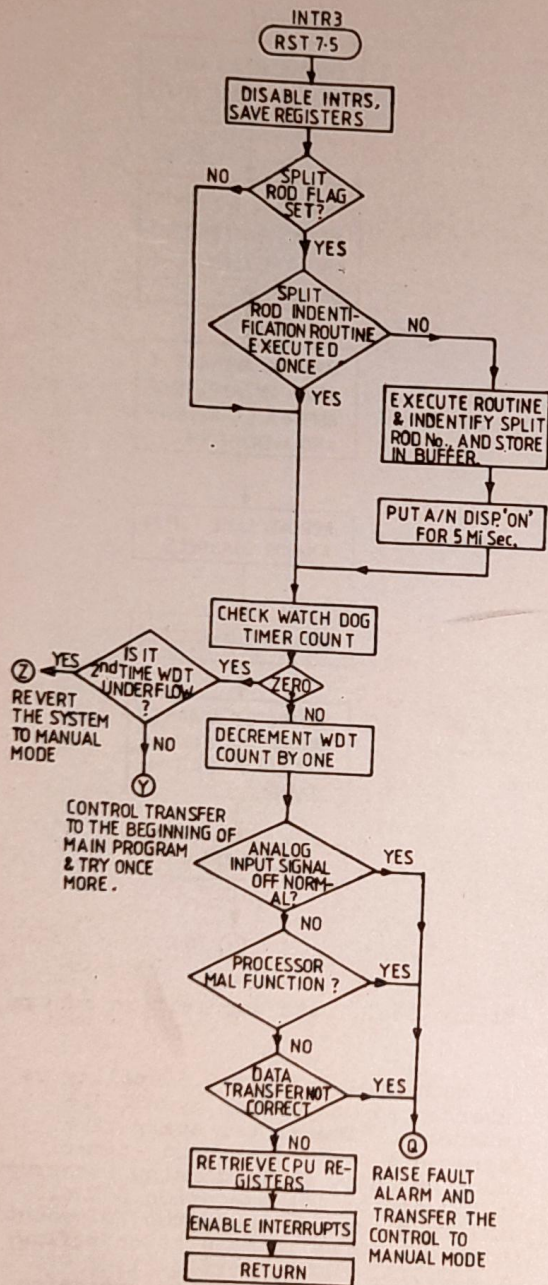


Figure 3(b). Timer interrupt service routine.

(ii) Co-incident high signals of a unique pair of detectors correspond to the existence of fuel failure in a particular position (out of 180). All the fuel rod numbers 1 to 180 (01H to 0BEH in hexa-decimal) remain stored in a ROM table of two dimensional array of 20 x 19 elements. Suppose for the Nth fuel rod element the first detector is Ji and second is Ki then the address of the corresponding array element where fuel rod number is stored is -

$$\text{Offset} + J_i + 20 K_i$$

Content of this address can be any number 'N' from 01 HEX to 0BE HEX (i.e. 180). This number is utilised to further address a one dimensional array of actual fuel rod identification numbers, each number is in three characters-first is alphabet and the remaining two are numbers (i.e. for example Q11, J19 etc.). In this way each fuel rod identification number will occupy three memory locations or bytes. Therefore, the starting address of the Nth fuel rod number is -

$$\text{new offset} + (N-1) \times 3$$

Once this number is located and identified, it is stored in a memory buffer in proper format for refreshing of the A/N display, repeated at 100 Hz frequency. The display duty cycle is maintained at 10%. Main program sets a flag in an alarm status word in memory buffer when there is simultaneous high signal in any of the two detectors, meaning that fuel failure has occurred. If this flag is found to be set, then only the utility program of this interrupt is activated for locating and identifying the exact fuel rod number, otherwise it remains dormant.

(iii) The third very important task which is taken care under this utility is regarding the software diagnostic checks. All these checks are carried out once every 2.66 milli-seconds, which include--execution of certain instructions on processor, memory to CPU and CPU to memory data transfer, and magnitude checking of input analog signals which should not be excessively high or excessively low. Mal-operation in any of these shall lead to alarm annunciation and reverting the system to manual mode.

The trap interrupt line of 8085, which otherwise is normally used for advance sensing of power failure, is made use of for routine manual diagnostic checks at suitable time intervals. This routine checks the value of set points,

tests almost all the categories of 8085 instructions by executing and checks the level of signals from input signal conditioning circuitry. In this process if any error is detected, the system comes to 'Halt' state and Panel off-normal indication appears, otherwise a green display remains 'ON' for few seconds indicating that the system is healthy. The termination of this routine transfers control to the beginning of operating system in the main routine.

The above facility is introduced to carry out a sort of preventive maintenance check to know any malfunctioning in the system in advance.

#### (c) Fault-Tolerance:

Fault tolerance is correct execution of any specified algorithm in the presence of defects. It can be achieved by redundancy in either the software or hardware of the system (2). The case of software redundancy is, for example, in A/D conversion where each input channel is sampled many times at the rate of 500 samples per sec. (200 milli second per sample) and averaged out so that any transient etc. on the analog input lines get filtered. In some other software or hardware failure also, fault tolerance is achieved by retrying execution after a small pause so that transient may possibly die out. If there is no success in this also, then the control is transferred to the manual mode.

#### (d) Power supply:

The reliability of instruments and control power supply is always ensured in any nuclear power reactor. For example, in this particular case, the MA (Motor-alternator) set used for instruments power supply is having battery bank riding over the motor supply which is available from MG (Motor Generator) set; so that practically there is no chance of power supply failure for this micro-based system. On the mains failure battery bank will run the MA set.

### Conclusion

The complete operating system was written in assembly language to keep the speed of execution higher, while maintaining the efficient memory utilization. It is possible further to reduce the size of the RAM by modifying the routines used for A/D conversion and averaging.

All the functions were implemented by VLSI ICs and software routines, as far as possible and the component count was kept to the minimum to achieve better system reliability.

It was noticed that most of the errors are transient in nature, hence inclusion of retry owing to the transients obviated the difficulties.

Sophisticated data acquisition systems based on higher level languages like concurrent Pascal have also been designed and implemented using advanced development facilities (3).

### Acknowledgement

The author is grateful to Head, Reactor Maintenance, B.A.R.C., for the sanction of this project and his unceasing motivation and encouragement for the completion of this Project. Author is also highly indebted to Dr. D.C. Surana, Professor & Head, Department of Electronics and Communication Engineering, University of Jodhpur, Jodhpur for his fruitful discussions which helped for the preparation of the manuscript for this paper.

### References

- (1) Intel 8080/8085 family User's manual, 1979.
- (2) Siewiorek, D.P. 1984: "Architecture of Fault-Tolerant Computers", Computer, Vol.17, Number 8, P.9.
- (3) T.L. Huang, R.L. Gulbranson and J.M. Finn, 'A higher level language data Acquisition System (II)- the development system', 3rd Biennial Conference on Real-time Computer Applications in Nuclear and particle Physics, Berkely, CA, May 16-20, 1983, USA.