

Operating System Concepts

(Memory management: Segmentation and Paging)

Slides Set #16

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Segmentation....

say address is 16 bit
3-bit , 13-bit offset
seg. no. (0-7) (0-8191)

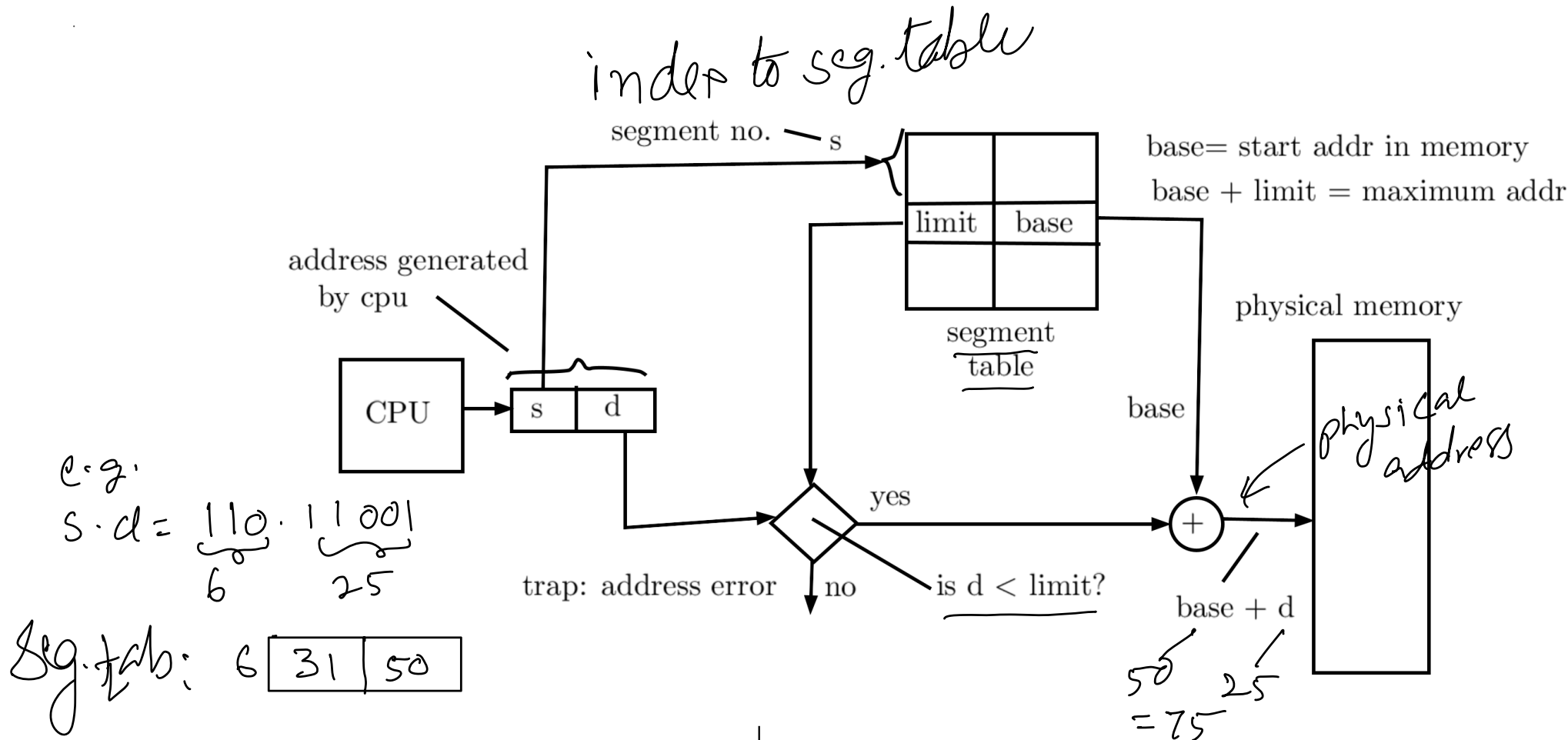
- ▶ Each segment has a name and a length. At run time, the CPU generated addresses specify both the segment name and the offset within the segment.

$\langle \text{segm_no.}, \text{offset} \rangle$

For example, a C compiler will create separate segments for the following:

- The code (i.e., main() and functions),
- Global variables,
- The heap – from which memory is allocated,
- The stacks used by each thread,
- The standard C library.

Segmentation Hardware



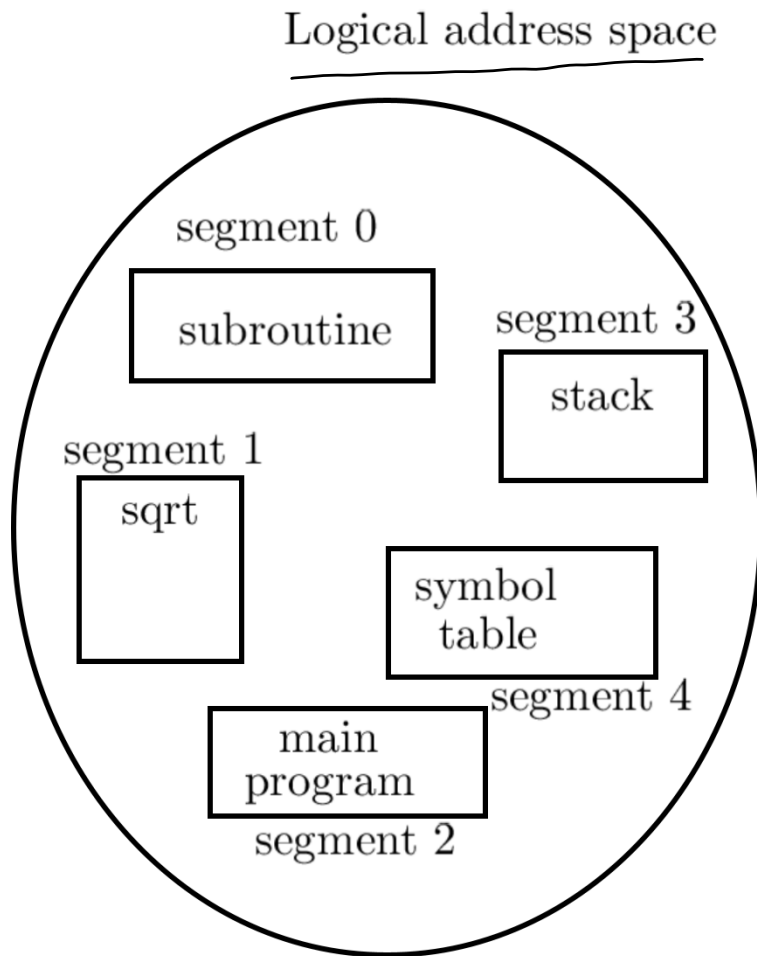
- ▶ Although the programmer can refer to objects in the program by a 2-dimensional address, the actual physical memory is still a 1

dimensional sequence of bytes.

- ▶ The use of a segment table is illustrated in Figure

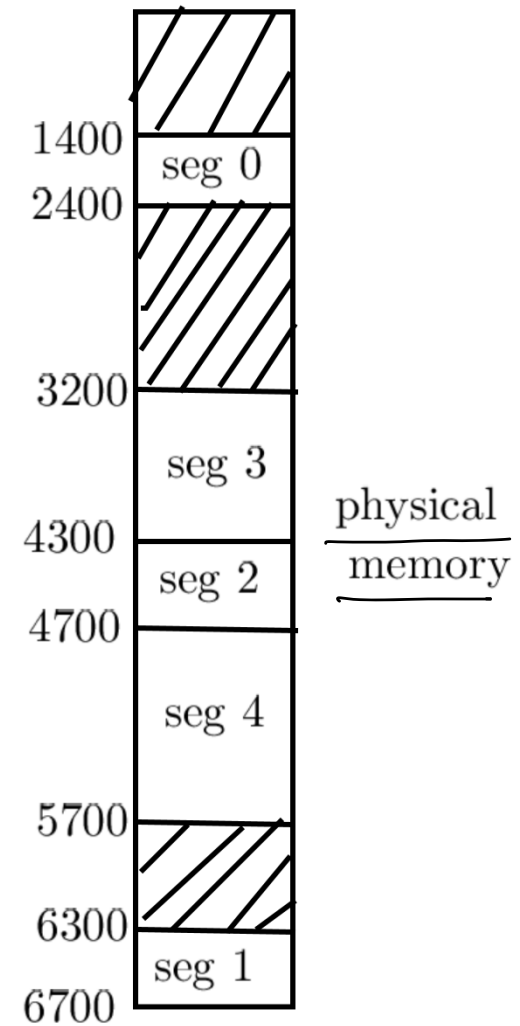
Segmentation Hardware...

Consider the situation of five segments numbered from 0 through 4.

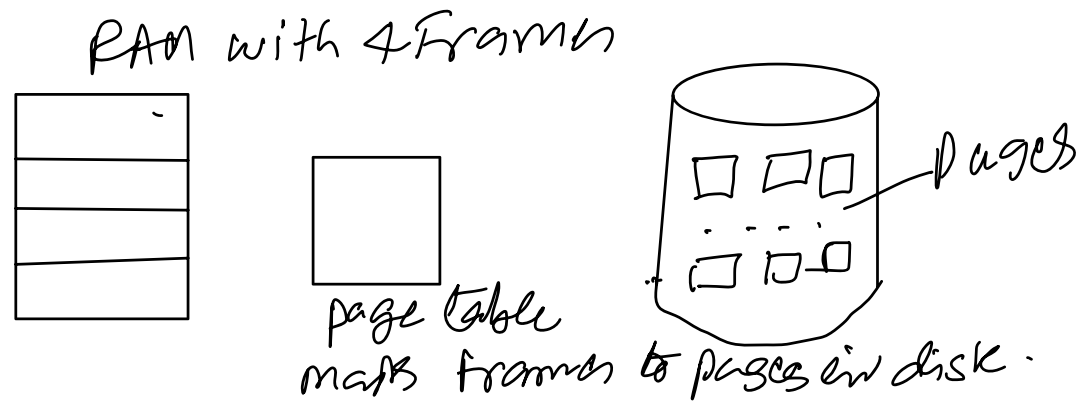


	limit	base
0	1000	1400
1	400	6300
2	400	4300
3	1100	3200
4	1000	4700

segment table



Paging



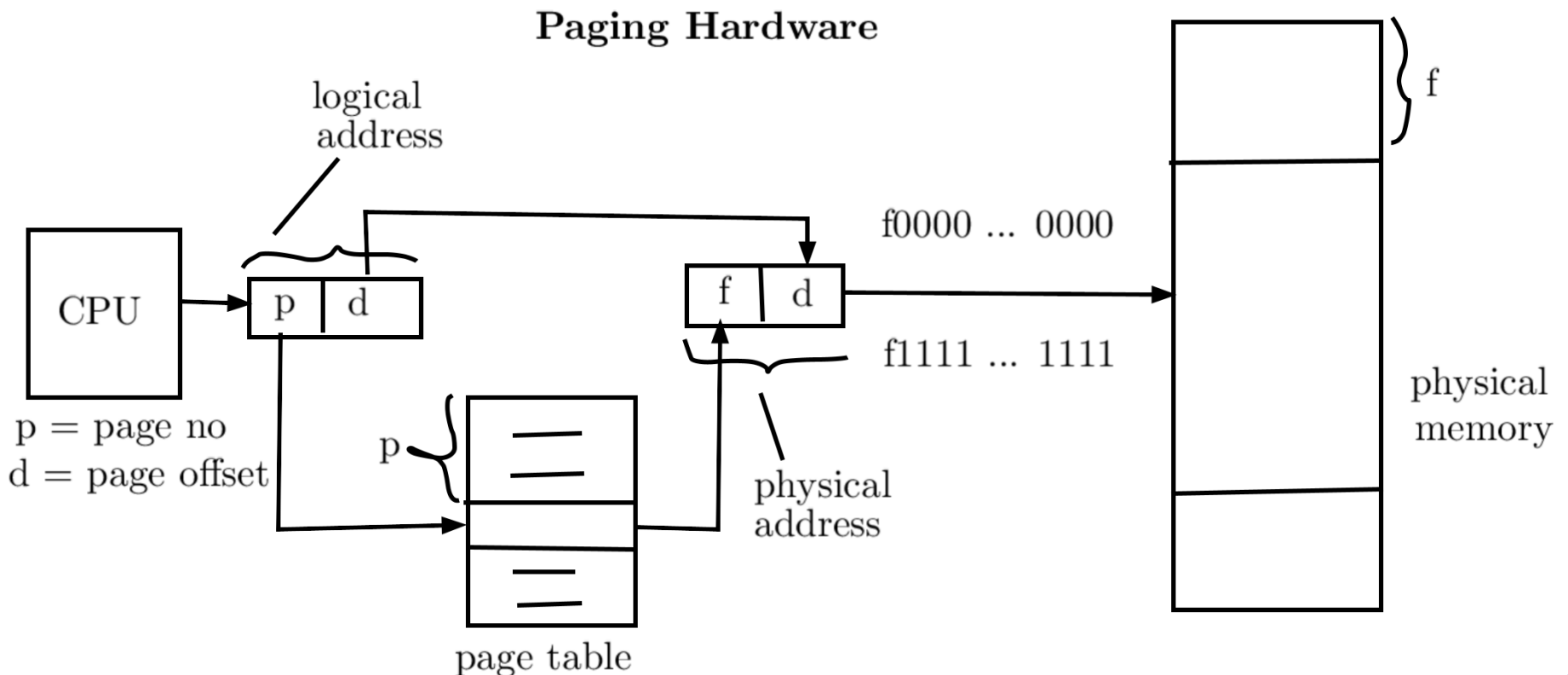
- ▶ Segmentation permits the physical address space of a process to be **non-contiguous**.
- ▶ Paging also offers this advantage. However, paging avoids external fragmentation and the need for compaction,
- ▶ The backing store has the same fragmentation problems discussed in connection with main memory,
- ▶ Because of its advantages over earlier methods, paging in its various forms is used in most operating systems,

Say: CPU address = 32 bit
Pages = $2^{12} = 4096$ (0-4095)
one page = $2^{20} = 1\text{MB}$
Say, RAM = 256 MB, \therefore 256 Frames

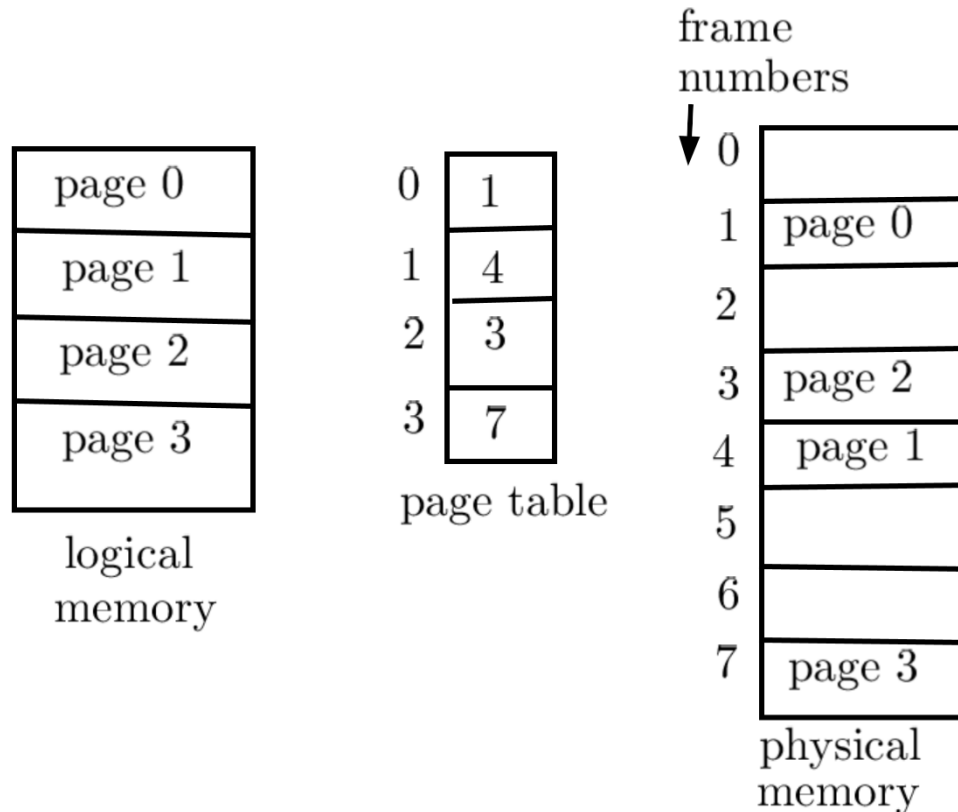
SO max. prog. size =
2¹² pages
and max. 256 pages
can be in RAM

Paging: Basic method

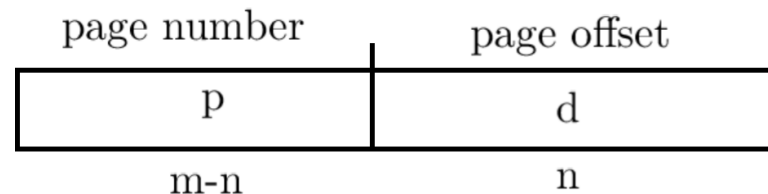
- ▶ **Basic Method:** The basic method for implementing paging involves breaking physical memory into fixed-sized blocks called **frames**
- ▶ For example, the logical address space is now totally separate from the physical address space, so a process can have a logical 64-bit address space



Paging model of logical and physical memory



The page size (like the frame size) is defined by the hardware. The size of a page is a power of 2, varying between 512 bytes and 1 GB per page. Thus, the logical address (2^m locations, and length= m bits) is as follows:



$p+d = \text{physical addr}$
 $\Rightarrow m-n+n = m \text{ bit}$